Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1734252	memory cell and array and address and buffer and latch and (address same detect$3) and (address same different)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:46
L2	175	1 and (control same circuit) and (timeout near circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:47
L3	678	1 and (control same circuit) and (timeout with circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:47
L4	98	3 and (cycle with operation) and (start with time)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:48
L5	70	4 and (end with operation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:49
L6	49	5 and (address with buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:49
L7	44	6 and (next with cycle)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:49
L8	1	1 and takeuch-yoshiaki.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:51

L9	60176	1 and "365"/$7.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:51
L10	6	9 and 7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:53
L11	397	1 and (row with buffer) and (column with buffer) and (CE with buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:54
L12	20	11 and (WE with buffer) and (first with (row same latch))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:54
L13	11	12 and (second with (row same latch))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:55
L14	9	13 and (column with latch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:55
L15	9	14 and (chip with enable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:55
L16	1	15 and (ATD with 'AND')	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:56

L17	154	11 and (internal with CE)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:56
L18	5	17 and (timeout with circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:57
L19	154	17 and (row with buffer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:57
L20	55	19 and (end with operation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:58
L21	21	20 and (start with operation)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:58
L22	0	21 and 365/ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:59
L23	0	21 and 365/7.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 09:59
L24	20	21 and "365"/$7.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 10:00

L25	37	(memory and cell and array and (address buffer) and (latch circuit) and (address transition) and (control circuit) and (timeout circuit) and (start time) and (end with operation) and (next cycle)). clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/03 10:02